ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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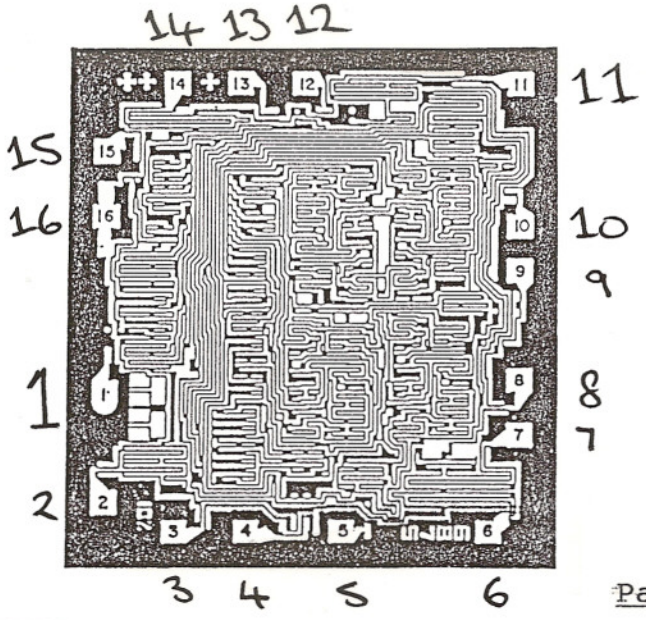
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function	Pad	Function
1	PRESET ENABLE	9	RESET
2	Q4	10	UP/DOWN
3	P4	11	Q2
4	P1	12	P2
5	CARRY IN	13	P3
6	Q1	14	Q3
7	CARRY OUT	15	CLOCK
8	V_{SS}	16	V_{DD}

Topside Metal: Al
Backside: Si
Backside Potential: Vdd
Mask Ref: 6875
Bond Pads (Mils): 4 x 4

APPROVED BY:	**DIE SIZE (Mils): 94 x 84**	**DATE: 3/13/00**
MFG: Harris	**THICKNESS: 20**	**P/N: CD4516B**

DG 10.1.2
Rev A 3-4-99